UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,743	01/29/2004	Marco Pasotti	856063.762	4907

38106 7590 06/27/2006

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,743	PASOTTI ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8 and 10-15* is/are rejected.

7)☐ Claim(s) *2,4,9,16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/05/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1 – 3 and 5 – 9, objected to because of the following informalities: Acronyms used in the claims should be spelled out before their first appearances. Appropriate correction is required.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 10 – 12 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14 and 15 of copending Application No. 10/748697 in view of Wong et al (US Patent No. 6,330,185, hereinafter "Wong").

4. Claim 14 of the copending application claims a memory system, comprising:

a memory module (a plurality of memory modules);

a power block (a plurality of charge pump circuits); and a

power management arbiter (an arbiter) coupling the power block to the memory module, the arbiter configured to distribute supply voltages from charge pump circuits to memory modules.

However, the copending claim 14 does not claim that the memory module comprises a non-volatile memory block. Nor does not claim sharing of a single charge pump among flash memory modules. On the other hand, Wong disclose a flash memory system (figure 1) where a single charge pump (150) is shared among flash memory modules (132).

It would have been obvious to one of ordinary skill in the art, having the teachings of the copending claim 14 and Wong before him at the time the invention was made, to share a single charge pump in the memory device of the copending claim 14 to provide for a uniform voltage source when accessing memory cells (Wong col. 3, lines 14 – 17).

5. With respect to claim 11, Wong discloses a plurality of flash memory modules having a multi-bank configuration (figure 1, 132).

6. With respect to claim 12, the power management arbiter comprises an order block configured to order requests for the memory modules (copending claim 15, sorting block).

7. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 14 of copending Application No. 10/748697 in view of Wong as applied above and further in view of Allen et al. (US Patent Application Publication No. 2003/0154430, hereinafter "Allen").

The copending claim and Wong disclose all of the limitations of instant claim 10 as discussed above. However, they do not disclose a memory system that is integrated into a single chip with a microprocessor as claimed in claim 1. On the other hand, Allen discloses that in automotive electronic control units, higher performance requirements have led to the use of higher end CPU which are typically embedded into a single chip that includes on-chip flash ROM (page 1, paragraph 2). It would have been obvious to one of ordinary skill in the art, having the teachings of Cernea (or Wong) and Allen before him at the time the invention was made, to integrate the flash memory system into a single chip with a microprocessor, to be used for automotive applications.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 3, 5 – 8, are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 3 require an order block configured to order requests for memory blocks following certain rules. However, the rules are not specified. Status of the request and priority information are not rules.

11. Limitations "said code port CP", "said second data port DP", "said third FP port" and "said second code port CP", and "said FP" port, in claims 5 – 8, respectively, lack proper antecedent bases in the claims.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Cernea et al. (US Patent No. 5,693,570, hereinafter "Cernea").

Cernea discloses a memory system (figures 1 and 2), comprising:

a memory module (20), the memory module comprising a non-volatile memory block (30) comprising a plurality of flash memory modules having a multi-bank configuration;

a power block (464); and a

power management arbiter (462 or 46) coupling the power block to the non-volatile memory block, the arbiter configured to provide charge pump sharing among flash memory modules in the non-volatile memory block from a single charge pump in the power block.

14. Claims 10 – 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong.

15. With respect to claims 10 and 11, Wong discloses a memory system (figure 1), comprising:

a memory module (100), the memory module comprising a non-volatile memory block (110) comprising a plurality of flash memory modules (132) having a multi-bank configuration;

a power block (150); and a

power management arbiter (120-1 – 120-N, collectively) coupling the power block to the non-volatile memory block, the arbiter configured to provide charge pump sharing among flash memory modules in the non-volatile memory block from a single charge pump in the power block.

16. With respect to claim 12, the power management arbiter comprises an order block configured to order requests for the memory modules in the non-volatile memory block (write circuits process requests in order).

17. With respect to claim 13, the power management arbiter further comprises a programming circuit having a multiplexer receiving as an input a voltage (120-1 receives Vcp and Vrp) from a voltage regulator and having an output coupled to a row decoder (VR1) for providing a read voltage to memory matrix rows, and a program switch coupling an output from the charge pump to a column decoder (VC1) for biasing memory matrix columns in the memory modules with a voltage generated by the charge pump.

18. With respect to claim 14, the system further comprises a testing block (125) coupled to the power block and the power management arbiter and configured to provide external access for testability.

19. With respect to claim 15, the microprocessor is configured to test the memory system (col. 3, lines 29 – 37), and wherein the testing block further comprises an analog-to-digital converter (col. 6, lines 56 – 65) for enabling access by external analog test equipment.

20. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Eckert et al (US Patent No. 5,889,303).

Eckert et al. disclose an embeddable flash memory system (figure 12), comprising a non-volatile memory (202, 204) for non-volatile storage of code, data, and bit-streams for embedded FPGA configurations (this is intended use language, EEPROMs are inherently capable of storing code, data, and bit streams), the system integrated into a single chip (200) together with a microprocessor (206) and having a modular array structure comprising a plurality of memory blocks, wherein a power block comprising charge pumps (208) is shared among different flash

memory modules (202 is equivalent to flash memory, it supports block erase like a flash EEPROM, see col. 3, lines 5 – 7) through a PMA arbiter (circuit in 208 that distributes power).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cernea or Wong in view of Allen.

Cernea and Wong independently disclose a flash memory system having a modular array structure where a charge pump is shared among flash memory modules. However, they do not disclose that the memory system is integrated into a single chip with a microprocessor. On the other hand, Allen discloses that in automotive electronic control units, higher performance requirements have led to the use of higher end CPU which are typically embedded into a single chip that includes on-chip flash ROM (page 1, paragraph 2). It would have been obvious to one of ordinary skill in the art, having the teachings of Cernea (or Wong) and Allen before him at the time the invention was made, to integrate the flash memory system into a single chip with a microprocessor, to be used for automotive applications.

Allowable Subject Matter

23. Claims 2, 4, 9, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. Claims 17 – 20 are allowed.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Woo H. Choi
June 20, 2006